Computer-aided technique for defect and project rules inspection on PCB layout image

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Abstract: *A technique of PCB layout optical inspection based on image comparison and mathematical morphology methods is proposed. The unique feature of the technique is that the inspection is performed at different stages of image processing. The presence of all layout elements is checked up, then positions of found elements and their conformity to project rules are verified, the breakouts and shorts are found. The inspection of mousebits, spur and pinholes on conductors is also carried out.*

Keywords**:** PCB, layout inspection, fault search and classification.

I. INTRODUCTION

An important problem in manufacture of a microelectronic equipment is the printed circuit board (PCB) layout inspection. The non-contact optical methods is widely used the control of PCBs.

An object for the inspection will be the image of PCB layout. The problem definition is the following. The raster pattern of the PCB layout and the set of project rules are given. The artwork image of PCB layoutcan be given in addition. It is required to check whether the PCB elements meet the given project rules, and to described their defects.

As elements on the PCB layout image we will define the contact pads, conductors, control points and the service information in the character form. The defect under inspection is the deviation of layout elements on PCB

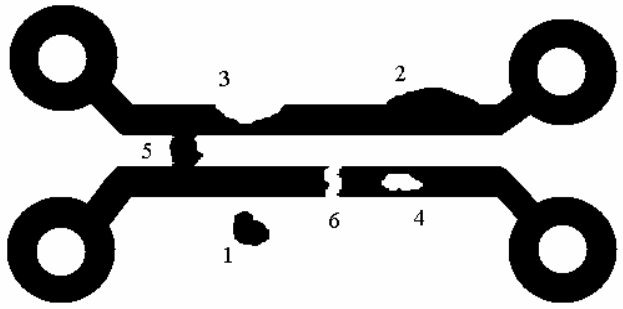

Fig. 1 - Example of a PCB layout defects: 1) spurious copper; 2) spur; 3) mousebit; 4) pin hole; 5)short; 6) breakout.

layout image from the project documentation owing to errors by manufacture, such as discrepancy of temperature and manufacture time modes, mechanical misregistration, etc. The example of some defects is replaced on fig.1. The defects can be divided into the following kinds: spurious copper (1), spur (2), mousebit (3), pin hole (4), short (5), breakout (6), discrepancy of the conductor minimal width and the minimal distance between conductors to project rules, absence or displacement of any element [1].

Various automatic algorithms were developed to the inspection of PCB layout over different manufacture phases with use of light, fluorescent light and x-ray. They can be separeted into three categories: reference based, project rules verification based and hybrid algorithms [1-4].

The reference based algorithms compare reference and test images of PCBs directly or use a set of models with the advance informative attributes as the reference. At comparison with the reference it is possible both pixel by pixel comparison of the test image with the reference sample image (subtraction of images), and allocation with the subsequent comparison of information attributes of PCB layout elements [1, 5 - 7]

The model based algorithms, such as parse, algorithm of graph matching, algorithm of attributed graphs make comparison of layout elements as a set of the models which describe the reference.

The automatic inspection algorithms, which are not use the reference, check elements of layout on conformity to project rules of a microelectronic product, such as the minimal and maximal width of conductors and distance between them, the minimal and maximal diameter of apertures on object, the curve of a conductor, the inspection of conductors termination rules, etc [8]. That algorithms often use operators of mathematical morphology, such as “ERODE” and “DILATE”. Algorithms based on the analysis of elements border can also be applied. After obtaining of the border there is made verification of an element by movement along its border with the inspection of special parameters. Element edge lengths coding can also be applied to search of defects [1].

The hybrid inspection algorithms are based on both comparison and project rules verification methods [1, 9 - 11].

Application of the reference for the layout inspection allows to find quickly and correctly faults like spurious copper, spur, mousebit, pin hole, short, breakout. The additional analysis of the received set of the faults allow us to find the absence or displacement of elements. The main lack of the given approach is dependence of faults localization accuracy on overlapping accuracy of reference and test images. The overlapping accuracy depends on scaling and turn operations of the test image,

its preliminary processing and binarization. For the inspection of the minimal conductor width and the minimal distance between conductors we shall use the algorithm based on morphological operators “OPEN” and “CLOSE”.

In the paper we offer new technique of PCB inspection with using advantages of the image comparison approach and the method based on mathematical morphology operators. The PCB layout inspection technique represents stage-by-stage procedure. In the beginning preliminary image processing is made. The presence of all elements on the PCB layout image is checked up at this stage. The output of this stage is the binary PCB layout image with corrected scale and rotation angle. At the next stage the search of defects is performed using method of comparison with the reference. The search can be carried out on the raster image or on its vector representation. The found defects are classified and their geometrical parameters are measured. At the last stage the search of defects with use of morphological operators "OPEN" and "CLOSE" is performed. Therefore we define regions on the PCB layout image, where project rules for the minimal width of a conductor and the minimal distance between conductors are not carried out.

The paper is organized as follows. In section 2 the technique of the defects search based on a method of comparison with the reference is offered. The search of layout defects is realized both for raster, and for vector representation of the PCB layout image. The method of classification of defects is offered. The technology of search of defects like a deviation of the minimal width of a conductor and the minimal distance between conductors from project rules is also considered.

II. DESCRIPTION OF THE TECHNIQUE OF PCB LAYOUT INSPECTION

A. Preliminary image processing

Preliminary processing of the test image consists of binarization, corrections of a rotation angle and scaling. The gray-scale picture received from an optical system is transformed to a binary image using the treshold Bts calculeted by the formula:

$$Bts = 2/3 * (Bmax - Bmin), \quad (1)$$

where Bmax and Bmin are the maximal and minimal values of brightness of the image.

The test image can have distortions of scale and a rotation angle. Control points are used To correct these distortions. The control points are selected on the reference image, and then the search of these points is performed on the test image. Finally the correction of the rotation angle and scale is carried out.

Search of all contact pads is made on the binary image, and lists of contact pads for the reference and test image are formed accordingly. The reference and test lists are compared with each other, therefore presence of all elements on the PCB layout image is checked up, and finally verification of found elements position is performed.

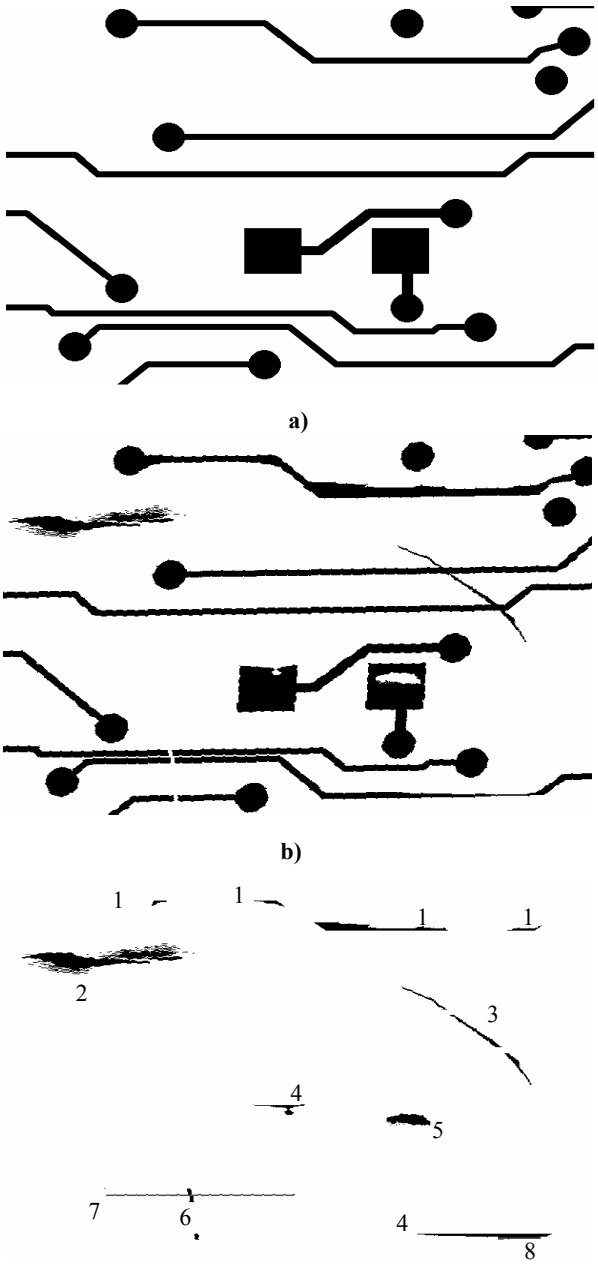

Fig. 2 - The reference PCB layout image (a); processing image (b); found defects (c): 1) spur, 2) spurious copper, 3) short, 4) mousebit, 5) pin hole, 6) breakout, 7) distance between conductors is less than project rules, 8) the width of a conductor is less than project rules.

B. The PCB layout inspection

After the preliminary processing the search of defects by a method of pixel by pixel calculations of XOR logic operation on reference and test images is carried out.

It is necessary to carry out the following tasks:

1. Find faults of the PCB by comparison a binary reference and test images.

2. Measure geometrical parameters of defect are: length, height and the area.
3. Classify faults as:
   - spurious copper;
   - spur;
   - mousebit;
   - pin hole;
   - short;
   - breakout

The vector description is made for each defect. On fig.2.a example of the reference PCB layout image are depicted. On fig.2.b one can see its image with defects and the deformed scale and the rotation angle. The result of defects search by means of operation XOR is shown on fig.2.c (defects are marked by numbers 1 - 6).

C. The inspection on the vector image of PCB layout

Search of faults like spur and mousebit on vector representation of the image of the PCB is realized on the basis of algorithms Weiler-Atherton and Margalit-Knott. For search of faults vector representations of reference and test images of PCB are used.

All elements on the image of the PCB are considered as polygons. First, a check of an intersection of reference and test polygons by the coordinates on the image is performed. If polygons are intersected, points of mutual crossing of the polygons borders are calculated and then tracing along borders of polygons is carried out for building of a required polygon. Tracing begins from an external point of local area of polygons. After the first point of edge crossing is reached, tracing is carried out on the internal side of the polygon formed by crossing of the edges of considered polygons in an opposite to initial one direction. After the second point of the polygons edges crossing is reached, procedure returns to the starting point of tracing on the external edge of a new polygon. Having defined thus coordinates of all points of a new polygon, we obtain vector representation of PCB defect.

Then the vector description of all found defects of the PCB is made.

D. The defect classification

After defect localization we determine which class of faults it belongs to. Classification is realized by means of the logical flags defining value of brightness for pixels of the found fault and the pixels around it. In table 1 the rules of classification is shown dependinging on various values of flags.

Let's consider the example of the defect on fig.3, where figure fragments of two direct conductors are represented. To each pixel on the image there corresponds as square. Pixels corresponding to conductors on the reference image are shown by grey color. Conductors are marked by numbers in the left top corner. The background is presented by white pixels. Pixels of defect have black color and are marked by small white squares. Pixels which border on defect, are marked by diagonal lines. It

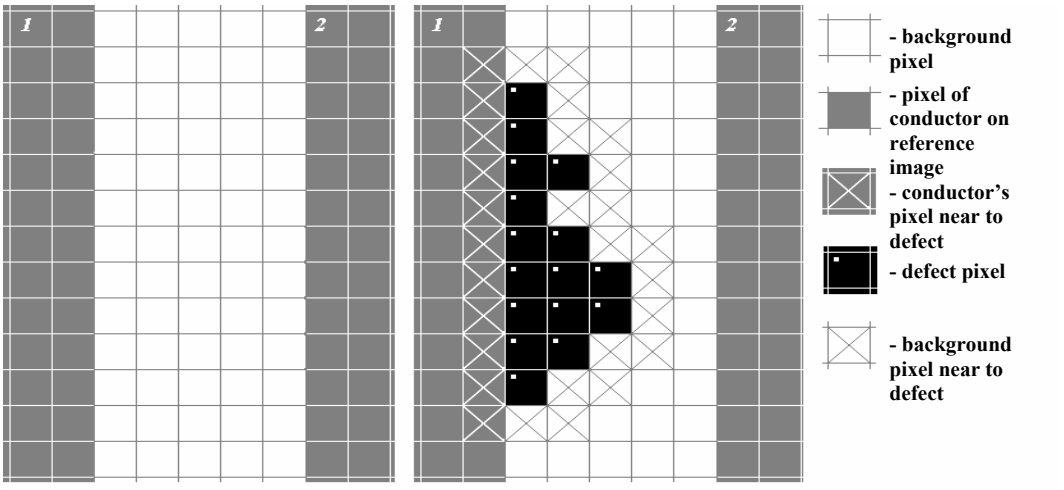

Fig. 3 - The defect classification: a) reference image, b) test image with defect.

Table 1. Fault type definition by logical flags

Logical flag				Type of defect
Is there the defect copper on background?	**Does the defect touch with copper?**	**Does the defect touch with background?**	**Does the defect touch only one conductor?**	
Yes	Yes	Yes	Yes	Spur
Yes	Yes	Yes	No	Short
Yes	No	No	Yes	Spurious copper
No	Yes	No	Yes	Pin hole
No	Yes	Yes	Yes	Mousebit
No	Yes	Yes	No	Breakout

can be seen that:

defect looks like a set of black pixels on a white background;

defect is adjoined with both black and white pixels of the image;

defect adjoins only to one element on the image (element 1).

According to table 1 the defect is classified as spur.

For faults like spur and mousebit the additional check is made: if the fault borders on two or more PCB elements on initial images, it belong to the class of short and breakout accordingly.

E. The inspection the minimal conductor width and the minimal distance between conductors

At the certain PCB manufacturing phase there is a necessity to check conformity of the minimal width of a conductor and the minimal distance between conductors to project rules. Localization of points on the image, where these project rules do not carry out, is made with use of mathematical morphology operators "OPEN" and "CLOSE" [12]. To define conductor regions with a width less than set project rules, the next formula is used:

$$\text{Rminwide}(A, B) = A - \text{OPEN}(A, B), \quad (2)$$

where A is the binary test image of the PCB, B is the round structuring element, which diameter is equal to the minimal width of the conductor according to project rules. Morphological operation "OPEN" has a property to delete those regions, which width is less than the structuring element. The result of the given operation is the set of image regions with width of a conductor less then minimal admissible on project rules.

For receiving of test image regions with the distance between conductors less then project rules we use the formula

$$\text{Rmindist}(A,C) = A - \text{CLOSE}(A,C) \quad (3)$$

where A are the binary test image of the PCB, C are the round structuring element, which diameter is equal to the minimal distance between conductors according to project rules. Morphological operation "CLOSE" has a property to delete those spaces on images, which width less than a structuring element. The result of the operation is a set of image regions with distance between conductors less then minimal admissible on project rules.

The example of the defects caused by discrepancy is project rules is shown on fig. 2.c: number 7 marks defect like distance between conductors having width less than project rules and number 8 marks defect like the conductors width is less than project rules.

III. CONCLUSION

Technique of PCB layout inspection based on image comparison and mathematical morphology methods is offered. The method of classification of defects on the basis of logycal flags is offered. As a result there will be checked up the presence of all elements on the PCB, verification of found elements position and their conformity to project rules, the presence of breakouts and shorts on the PCB. The inspection of mousebits, spur and pinholes on conductors is also carried out.

The proposed technique is realized in the computer-aided system of the PCB layout inspection. The PCB layout inspection system allows carrying out automatic inspection of conformity contact pads on the tested PCB (on types and an arrangement) to data in Gerber format of the reference PCB. Automatic inspection of conductors faults. The system is realized under OS Linux in the programming language C++.

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The research is partially supported by the Belarusian Republican Foundation of Fundamental Research, grants T04-219 and T04M-119.