FPGA Implementation of Nonlinear Neural ADC-based Temperature Measurement system

Keywords: ADC, FPGA, Implementation, Measurement, Neural network, Nonlinear

1. INTRODUCTION

The extensive use of the digital solutions (DSP, Microcontrollers,…) in measurement and control has increased the linearity requirement on transducer output and other signal. These requirements are not always easily met, and are often possible only at the expense of other desirable transducer characteristic.

Many techniques have been proposed to provide linearization of transducer output, such as analog circuits, segment linearization, microprocessors and RAM [1]. Recently, the use of neural networks (NNs) to linearize the nonlinear characteristic has been proposed because they give good results [2-3], contrary to the classical electronic techniques, for which they are complex and limited to reduce the influence of perturbations [1]. Also, Flash ADCs analog to digital converters have been designed with NNs where the circuitry complexity was considerably reduced [4-7].

Field programmable gate arrays (FPGAs) belong to the wide family of programmable logic component [8], their densities are now exceeding 10 million gates [9]. FPGAs can be defined as a matrix of configurable logic blocks (combinatorial and/or sequential), linked to each others by an interconnection network that is also entirely reprogrammable.

FPGAs technology allows developing specific hardware architecture within a flexible programmable environment. This specificity of FPGA gives the designer a new degree of freedom comparing to microprocessors implementation, since the hardware architecture of the synthesized system is not imposed a priori.

A number of reasons can be pointed out as the motivation for building NNs in digital hardware; need for high processing speed, reduced cost for implementation and reliability. Considering the possible solution for a digital implementation, the FPGA solution is the most interesting taking into account the balance performance/price [10-11]. However, the main goals of this work is; the minimization of the neuron numbers for the 4-bit nonlinear analog to digital converter (NADC) model, the optimization of the synthesized NN circuit in view to FPGA-implementation and the design of the analog part and the very high speed integrated circuit hardware (VHDL) description program to realize 8-bit NADC using the 4-bit neural NADC.

The proposed circuit is realized on 50 MHz FPGA (SpartanII) from Xilinx. Moreover, the developed device can be easily modified, implemented and used in many fields of instrumentation systems and control algorithms.

2. 4-BIT NONLINEAR ADC MODELING

The used sensor for the temperature measurement is a thermocouple (type K). A thermocouple generates a voltage proportional to the measurement junction temperature at mV levels while the cold junction is constant. The corresponding characteristic is taken from Ref. [12].

The first idea which comes to mind in order to modelize a neural NADC with 4 bits is to choose a multilayer architecture with one hidden layer, an input and four outputs. This architecture has primarily two problems: difficult training because of the hard nonlinearity of the characteristic of the NADC and consumes many neurons and consequently an expensive implementation. This deals to choose a decentralized architecture where four NNs are chosen.

The global architecture has one input and four outputs when each output has its own NN. Each neural network is trained independently and depends on the significance of the bits. To simplify and optimize the FPGA implementation, the activation function σ chosen for each neurons in the whole architecture is the hyperbolic tangent with high slope equal to 30 ($\sigma(x)=\tanh(30x)$), in practice, this activation function is the heaviside function (comparator).

Input voltage V_{th} issued from the signal conditioning circuit is directly fed into the four NNs. The NNs are trained using the inverse sensor's characteristic in the range (0-V_{ref}) with V_{ref}=5V, where each output of NNs depends on the significance of the corresponding bit. Like any NN modelization, three phases are followed: learning phase, validation phase and testing phase [13-14]. The learning phase is realized with the backpropagation algorithm using Neural Network Toolbox of Matlab and follows a strategy to identify the neural network for every bit. The results of the learning phase are shown in Table.1, where 26 neurons are needed in the hidden layers.

After a minute observation and analyze of the NN weights file an appropriate architecture for the NN can be given in Fig. 1. The NN required to generate the NN_i (i=2, 3 and 4) can be deduced from the NN_1 in the proposed neural architecture, so, the hidden layer of higher significant bits are included in the lower significant bit (LSB only). Thus, the Eq. 1 can be written:

$$NN_{H4} \subset NN_{H3} \subset NN_{H2} \subset NN_{H1} \quad (1)$$

Where NN_{Hi} is the hidden layer of the NN_i and NN_1 corresponds to the LSB output. However, this proposed architecture provides simplicity and optimization and as shown in Fig. 1, NN_i can be partly found in NN_1. With this optimized architecture, the number of neurons in the hidden layer is reduced to 15 from 24 obtained in the initial architecture.

Table 1. Results of the decentralized architecture learning phase

Bit	MSB	LSB+2	LSB+1	LSB
ANN	ANN_4	ANN_3	ANN_2	ANN_1
Neurons	1	3	7	15
Iterations	0	$4.5x10^3$	$2x10^5$	$3.2x10^6$
MSE	–	$5x10^{-6}$	$2.8x10^{-5}$	$4.7x10^{-5}$

3. REALIZATION OF THE 8-BIT NADC

Fig. 2 gives the basic configuration for the 8-bit NADC using two 4-bit NADC. For an analog input V_{th} lying in the full scale range of 0-V_{ref}, the first nonlinear analog to digital conversion is made and the most significant 4-bit digital outputs are determined. The $NADC_2$ gives the least significant 4-bit output to the same analog input V_{th} in the full scale range of 0-V_{ref2}, where V_{ref2} is a tension delivered by the commutable reference voltage circuit (CRVC). A correction digital circuit is used at the NADC outputs to overcome the glitches problems.

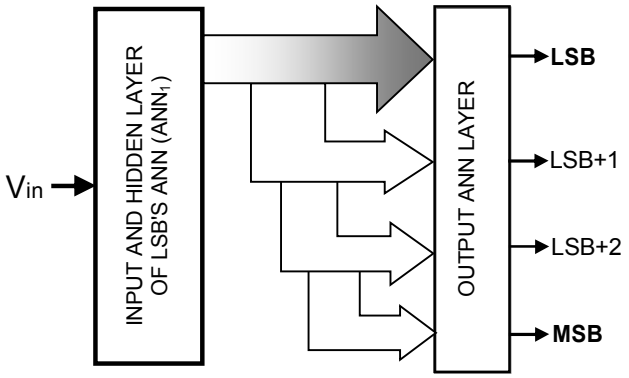

Fig. 1. Optimized ANN architecture

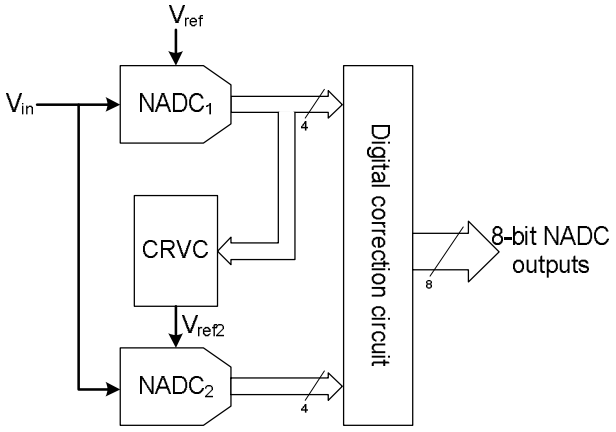

Fig.2. Basic configuration of the NADC

4. FPGA IMPLEMENTATION

Three different essential blocks can be distinguished in the functional diagram of the proposed FPGA-based NADC which are namely:

- The ROM block contains the obtained synaptic weights in the learning phase for the two NADCs.
- The output layer of the NADC; the architectures of the two NADCs are the same, they differ only in the synaptic weights values [15].
- Control unit bloc: this important circuit controls the whole functioning of the NADC.

More explanation about the analog implementation of the $NADC_1$ and $NADC_2$ can be found in Ref. [16].

The design approach was modular to accommodate higher order problems with increased resolution in the digital implementation [17].

5. SIMULATION AND TESTS RESULTS

The different synthesized modules are described with VHDL and synthesized with Precision Synthesis® Software. After placement and routing in ISE 7.1i® environment, the circuit is implemented in Xilinx Spartan II FPGA.

First the NADC has been designed and built, the next step is to realize tests to investigate the performances of the realized NADC. Testing of Analog to digital converters is classically composed of two successive and independent phases, the histogram-based test technique evaluating static specification and the spectral analysis technique evaluating the dynamic performances [18-23].

The first initial test carried out. By subtracting the D/A quantized output from the continuous analog input, a saw-tooth signal will be generated which represents the error voltage that result from the digitizing process.Figure 3 and Fig. 4

demonstrates the capability of the adopted NADC to reproduce the nonlinearities is evident, the done test show a difference between the analog values and those furnished by the neural model lower than ½LSB.

Fig. 5 shows the histogram with taking 5000 samples and a sine input signal with frequency of 1MHz. No outputs zero code has been observed on the histogram which indicates that there are no missing codes. Fig. 6 shows the error between the ideal model and the neural model output spectra with taking 5000 samples and a sine wave input signal with frequency of 5MHz.These tests illustrate that the corresponding output signal spectra for the ideal model and the neural model are very similar what leads to say that the characteristics of the two models are practically the same.

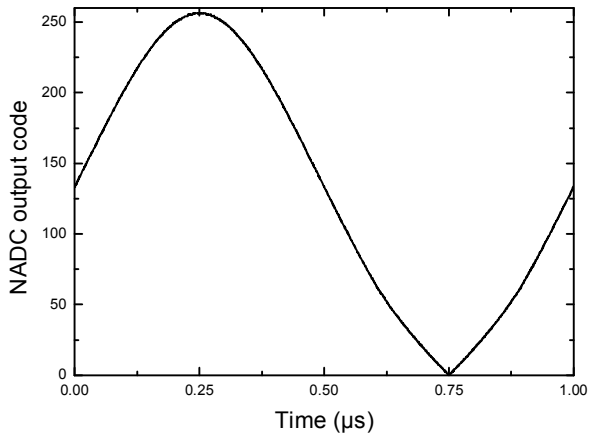

Fig.3. NADC response to a sinusoidal signal to the synthesized NADC.

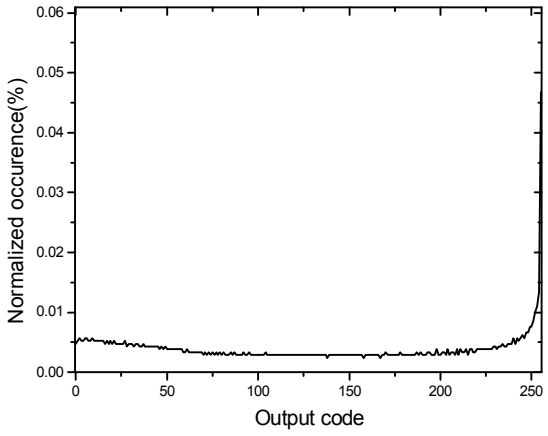

Fig. 5. Results of the histogram tests

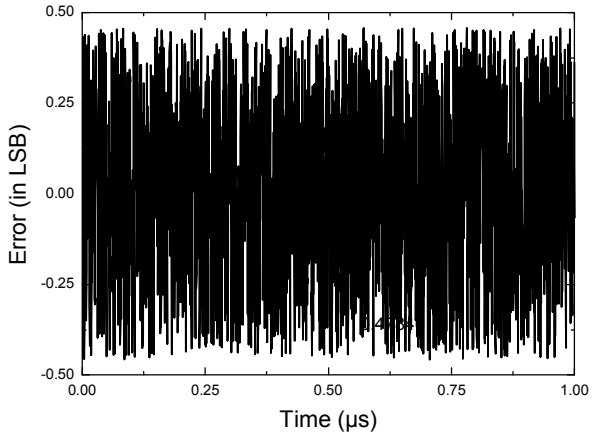

Fig. 4. Error between Ideal model between the digital characteristic and the analog characteristic.

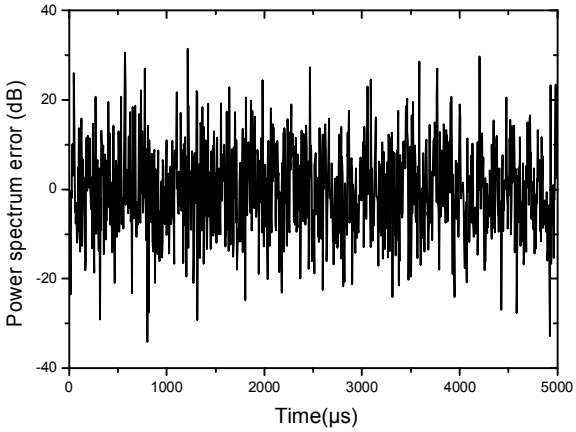

Fig. 6. NADC response to a sinusoidal signal and the difference and neural NADC output signal spectra.

6. CONCLUSION

The proposed modular-based design for the NADC has reduced the complexity to a greater existent compared of that of conventional linearization and flash analog to digital conversion circuits.

New optimal 4-bit neural NADC architecture is proposed to be developed on FPGA implementation. Only two hidden layers implemented in analog circuit and one hidden layer implemented in FPGA are needed to deliver the 8-bits of the whole NADC. The idea to use the CRVC circuit and the specified analog and digital neural implementations, which enable the user to set an appropriate circuit for any nonlinear application.

The temporal, statistical and spectral analysis were carried out to show the effectiveness and the aptitude of the synthesized NADC. This architecture based on FPGA could be expanded to realize others nonlinear NNs applications. In this paper, reconfigurability and adaptability were the main features of the hardware implementation. For furthers nonlinear applications based sensor correction only the weights, biases, and scaling parameters are needed for reconfiguring the CLBs without changing the basic design architecture.

The major contribution of this study :(i) the successful modelization of an optimal NADC, (ii) the successful implementation of the synthesized NADC in a FPGA chip.

7. REFERENCES

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